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Contributing Editors: Peggy Aycinena, Richard Goering,
Geoffrey James, Gary Smith
Editor-in-Chief: Gabe Moretti

DACeZine

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Peggy reports on the experiences of grad students at DAC.
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Peggy Aycinena
viewpoint

Richard Goering
DAC columnist

Limor Fix
general chair

Welcome to the New DAC Magazine - DACeZine!

The Design Automation Conference (DAC) continues to look for new ways to serve the changing needs of the electronic design community. DAC's new magazine, DACeZine, together with DAC's new and enhanced website (www.dac.com) will offer year round community resources for designers, technologists, academics and exhibitors, and everyone interested in electronics design.

Hope you will enjoy DACeZine, find it useful, and use it as channel to influence our community. Your feedback and involvement is welcome.

Best wishes,

Limor Fix
General Chair, 45th DAC

Gabe Moretti
editor

The Class of 2007: Workshop for Women in Design Automation at DAC
by Peggy Aycinena

The Workshop for Women in Design Automation, held each year in conjunction with the Design Automation Conference, welcomed six graduate students from four universities to the June 4th event in San Diego, thanks to the generous support of Cadence Design Systems, Magma Design Automation, Mentor Graphics, and EDA Confidential.

The sponsorships covered workshop registration, plus travel and lodging for those students who came to San Diego from out of town. Representing the University of Pittsburgh, Stanford University, U.C. Berkeley, and U.C. San Diego, these students are working across a range of research areas including circuit design and simulation, low power, reconfigurable computing, lithography and DFM. I had a chance to chat by phone with each of them recently, to talk about their work and their impressions of the Women's Workshop and DAC. It was a pleasure to speak to every one of them.

The students & their research ...

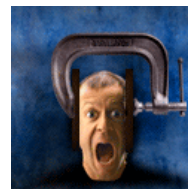
Sponsored by Cadence, Gayatri Mehta and Swapna Dontharaju both traveled to San Diego from the University of Pittsburgh, where Dr. Alex K. Jones is their advisor.

Verification gets 'intelligent' at DAC

The Design Automation Conference usually brings with it some "hot topic" in terms of startup activity and technology announcements. This year, I'm going to suggest, the hot topic wasn't a new or emerging EDA market segment. Instead, I think some of the most interesting technology on the exhibit floor and in the technical program had to do with bringing more intelligence and automation to IC functional verification.

Verification is an issue that's been around as long as there's been a Design Automation Conference. So why would functional verification be a hot topic now? The reason is that as transistor counts head for 65 nm and 45 nm and below, the functional verification problem grows exponentially. Functional verification already consumes much if not most of the design cycle, along with much if not most of the RTL code that's written these days.

The entire verification process has become a bottleneck that's desperately in need of intelligence and automation. Designers need to be able to quickly generate real-world test scenarios, put those scenarios into increasingly complex testbenches, determine how to test various blocks in the



Welcome to DACeZine

The Design Automation Conference (DAC) is the premier event for the EDA industry. It allows the EDA industry to showcase the newest technical innovations, to hear and discuss worldwide research efforts, and to provide a networking environment for EDA professionals and electronics designers. The latter should not be confined to a once-a-year event, and DACeZine, the Design Automation Conference magazine, aims to encourage the dissemination and sharing of news, opinions, and analysis of and about the EDA industry.

Following the success of DAC's newsletter, DACeZine offers expanded editorial coverage as well as an opportunity for its readers to interact using various channels, two of which - Viewpoint Articles and Letters to the Editor - are available immediately. DACeZine is meant to serve the electronics design and EDA community at large, and provide a venue for thoughtful analysis and discussion of topics relevant to the industry.

How it came about

The idea of publishing an electronic magazine was first suggested by Nanette Collins, DAC Public Relations Chair. The proposal received enthusiastic support from the DAC Executive Committee. Cook Design, together with MP Associates, have provided the technical expertise to design the format and enable the production and distribution of the magazine.

The DAC sponsors, ACM, IEEE, and EDAC have also supported the need to build an additional communication channel for our industry around its preeminent yearly event, DAC. Although the sponsors ably serve their own constituencies, they found it important to extend the conference's networking environment throughout the year.

The editorial team

The relationships built over the span of my career as an editor have given me the opportunity to assemble an impressive team of contributing editors. Richard Goering and Gary Smith, respectively the leading editor and leading analyst of our industry, are part of the team. They join Peggy Aycinena who brings both technical knowledge and humanistic sensitivity to her coverage. Geoffrey James contributes his knowledge of the business side of EDA and electronics design. His contributions will complete the balance of the magazine's contents. I am grateful to all of them for the interest and enthusiasm they have shown when approached with the

Mehta is going into her final year of grad school, while Dontharaju just defended her thesis in July. It's a huge accomplishment to complete a Ph.D., as all doctoral students know, and Dontharaju is delighted to be done. "The last few weeks of work and writing were very stressful, plus the defense," she said. "Many people say the defense of your thesis is just a formality after so many years of work and supervision from your advisor, but you never know. You still have to be very well prepared. Now that I'm finally done, I can start to do things at my own pace. I'll be working as an automation engineer at Intel in Oregon. The work will be challenging and very different from my research, and I'll have to learn a lot of things quickly. But I'm excited about the learning, taking on new responsibilities, and making a difference in my new group."

Gayatri Mehta still has a year to go for her Ph.D. Her research is in reconfigurable computing with a focus on the architecture and modeling of energy-efficient coarse-grained reconfigurable fabrics for embedded computing: "My area is mainly low power, which is one of the critical design concerns for mobile applications. I'm not working at the circuit level, but at a higher level of abstraction. I've designed a low-power parameterized fabric model and am using it to explore the architectural space in detail. I am also developing a tool to fully automate the design space exploration flow that will generate the fabric architecture based on the needs of the applications."

Since she's working on reconfigurable systems, I asked Mehta about the 'battle' between FPGAs and ASICs. "There are a lot of tradeoffs involved, so it depends on the application," she said. "Perhaps in 10 or 15 years, FPGAs might replace ASICs in a lot of applications, but for now they have higher power consumption and are a lot less desirable for mobile applications. A lot of research has been done over the past several years in this area, but it's going to involve a lot more effort to come up with power saving ideas for FPGAs."

[Read the rest of the article](#)

Guest
Speaker
viewpoint

What does DFM Mean for

design, control numerous simulation runs, apply formal verification, and use hardware-assisted verification with transaction-level interfaces. They also need better coverage metrics and quality control so they can determine when the job is done.

Some years ago, analyst Gary Smith put forth the vision of an "intelligent test bench" that would evaluate a design and apply the correct verification engines to various design blocks. As such, the intelligent test bench would provide an integrated, easy-to-use verification test suite that would avoid duplication and overlap. It couldn't be done from the register-transfer level alone, however, because it requires electronic system-level (ESL) information to work.

"This was a breakthrough DAC as far as functional verification was concerned," Smith said. "For the first time, we're seeing tools that can really carry out the full intent of the intelligent test bench." This is largely driven, Smith said, by the fact that verification is moving up to the transaction level, thanks to ESL-based methodologies. "Some companies popped up at DAC that are taking a look at how to do that," he said.

[Read the rest of the article](#)

idea of the DACeZine, and wish to thank both Peggy and Geoffrey for their past contributions to DAC's Newsletter. Additional editors and analysts will contribute their knowledge and opinions throughout the year. We will also feature technical contributed articles from designers addressing timely issues about methods and tools, including issues relevant to the theme of the upcoming DAC: wireless design.

Communication is a two way street

DAC is a service to the industry, and thus we need to listen to the professionals who work to keep EDA and electronics design exciting, challenging, and financially profitable. As such we will host a Viewpoint article in every issue. This issue features a Viewpoint by Rajeev Madhavan, Magma Design Automation Chairman and CEO, on DFM - one of my preferred editorial subjects for its complexity, ambiguity, and market uncertainty. The DACeZine will also have a Letters to the Editor section to allow for shorter contributions to the contents and directions of the publication. When necessary, answers to the letters will come from the appropriate member of the team (including our readers), since I do not (yet) hold the total knowledge of the industry within me. I encourage all of you to write, either a Viewpoint or a letter, and state your opinions on matters that impact our industry, the contents of this publication, or, for that matter, the publication itself. Send your letters to: dacezine@dac.com.

I hope you will enjoy the first issue and pass it along to your friends and colleagues. I am sure they will want to subscribe as well. They can do so by visiting the www.dac.com web page.

What does DFM mean for EDA?
Rajeev Madhavan
Chairman and Chief Executive Officer
Magma Design Automation, Inc.
San Jose, CA

DFM, does it mean, design for manufacturability or design for marketing? Recently it has been positioned as the next great inflection point in the electronic design automation (EDA) industry that will enable it to expand significantly with an entirely new segment. Just a few months ago as many as 27 different EDA companies offered DFM tools, 21 of which are startups, or so claimed John Cooley on DeepChip. All of the companies in the DFM market segment are trying to find a foothold and differentiate. In this mad scramble to appear to be first to market with a unique product, hype has gotten way ahead of product delivery. As a result, products that do not meet expectations confuse designers and DFM has come to mean design for marketing.

As a founder of three companies, and investor and mentor of many others, I can identify with the brilliant engineers who work so hard make these startups successful. When we founded Magma 10 years ago, we had carefully studied emerging deep submicron design challenges. We committed to integrating logic and physical design because we knew that that's what it would take. We succeeded -- and then some -- but it wasn't without more challenges than we could have ever anticipated.

I admit that there was a lot of hype around Magma in the early days, but that was for good reason. We were truly changing the way IC design was done so that we could ensure that our customers would achieve their performance, cost and time-to-market requirements. Today, all the large EDA companies claim to have an integrated flow.

[Read the rest of the article](#)